Hogan & Hartson 89165.0013 Daisuke KATO et al. Semiconductor Memory Device EV 325 217 341 US 18 Drawing Sheets; Sheet 1 of 18

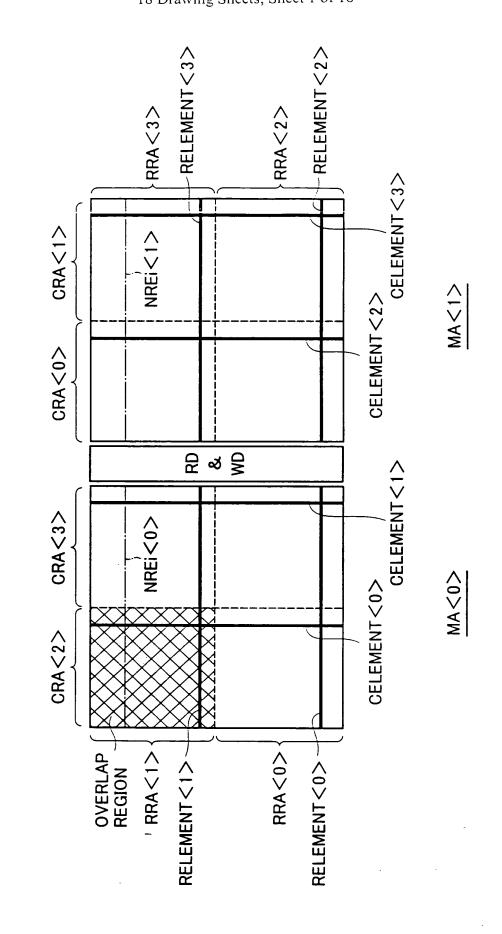


FIG. 1

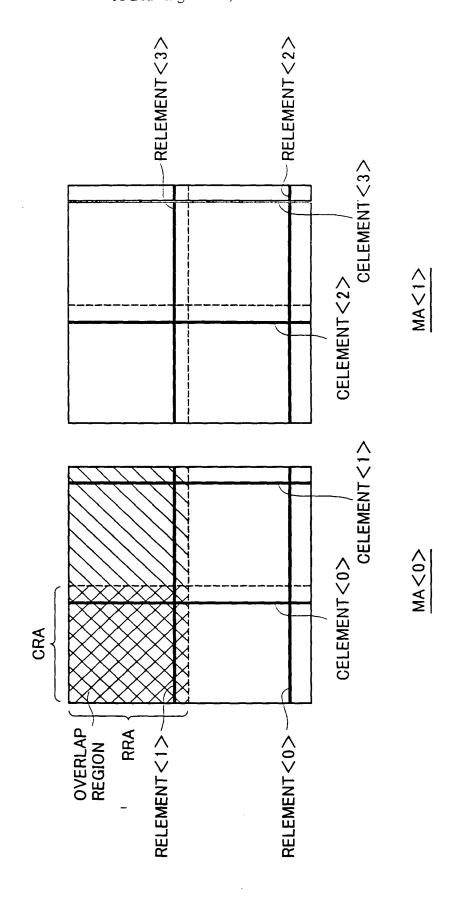
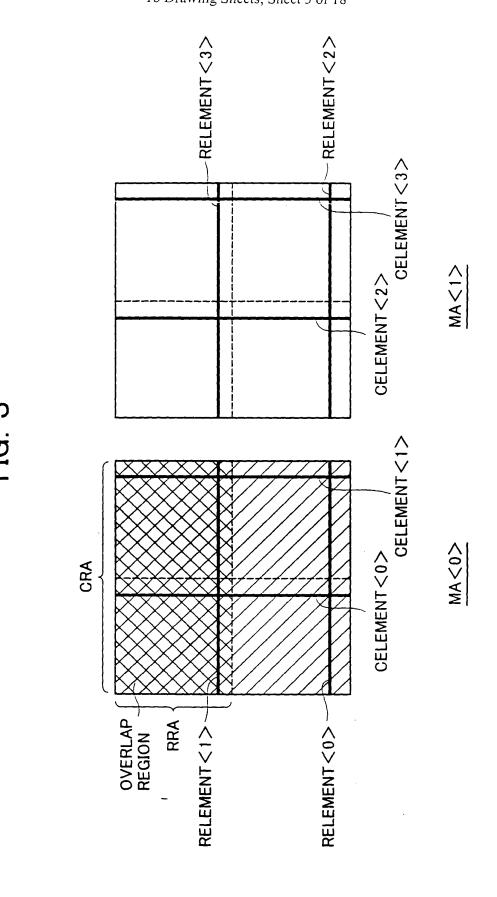


FIG. 2

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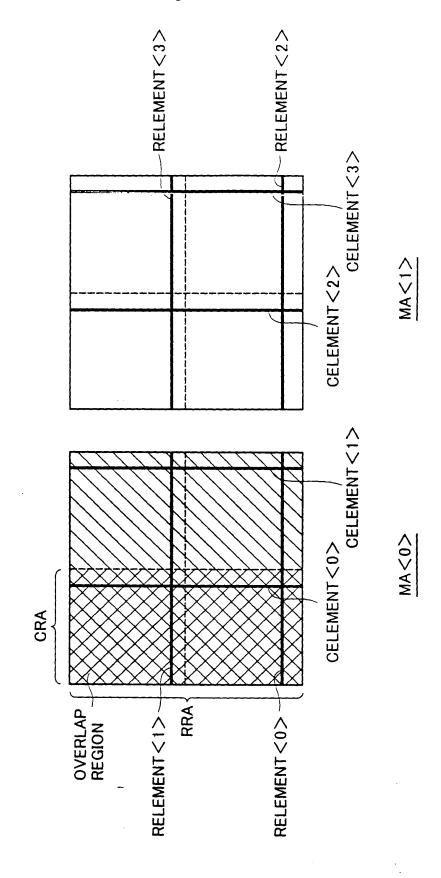


FIG A

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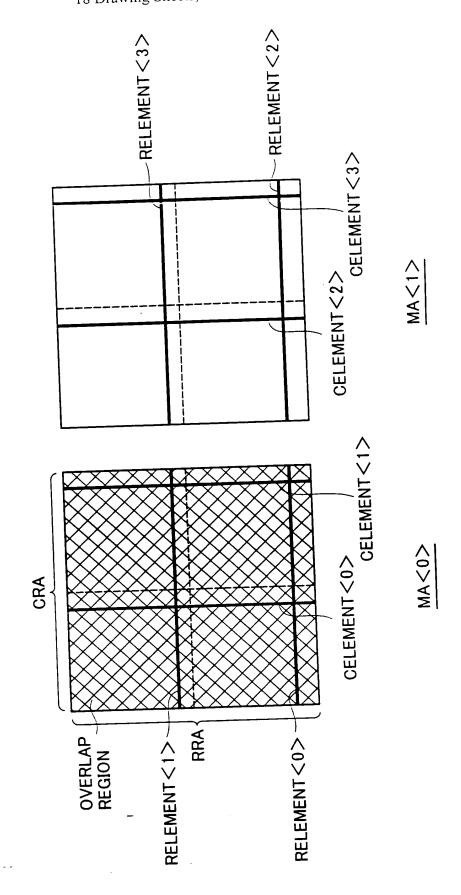
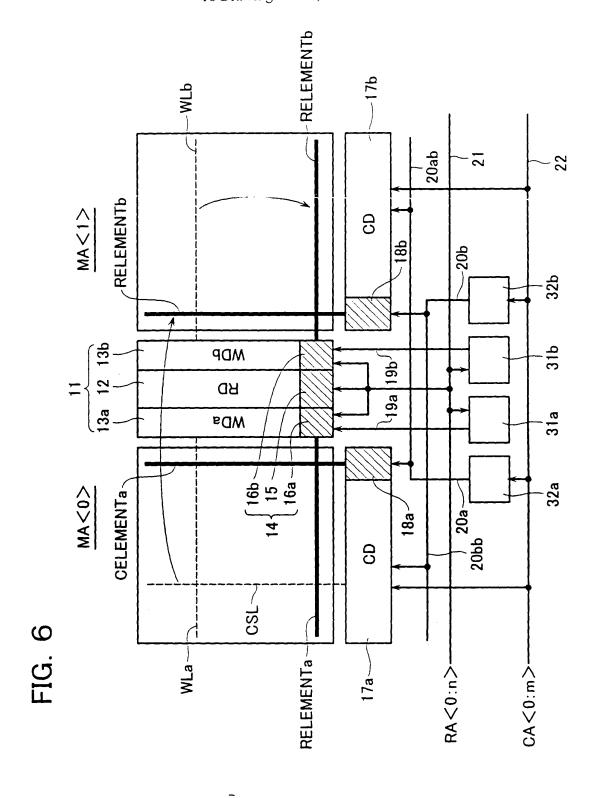


FIG. 5

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## FIG. 7

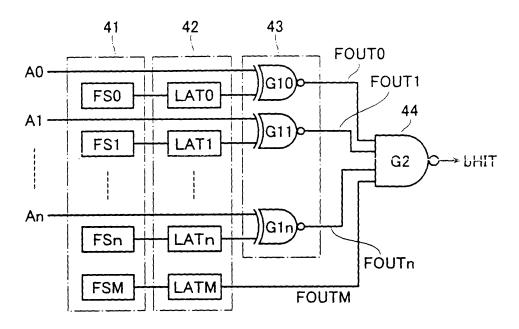
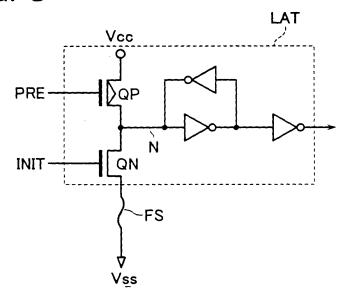
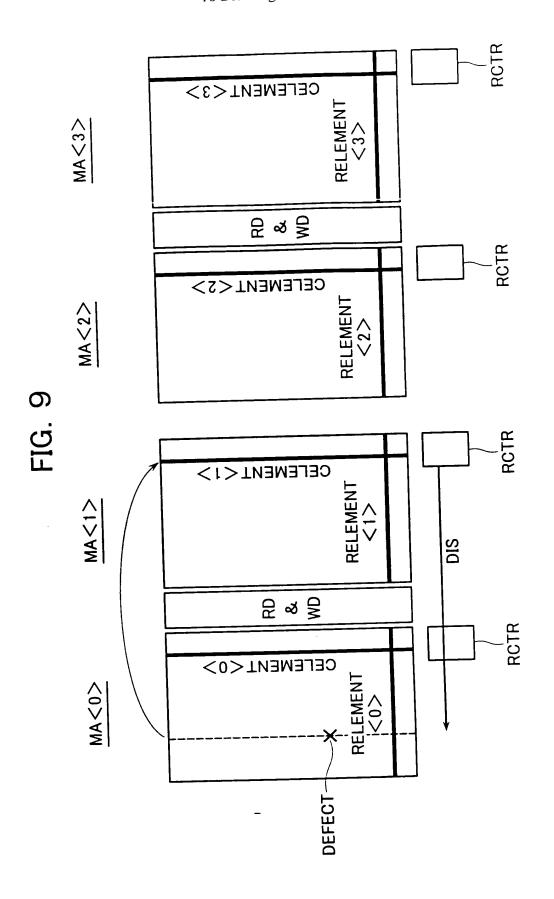


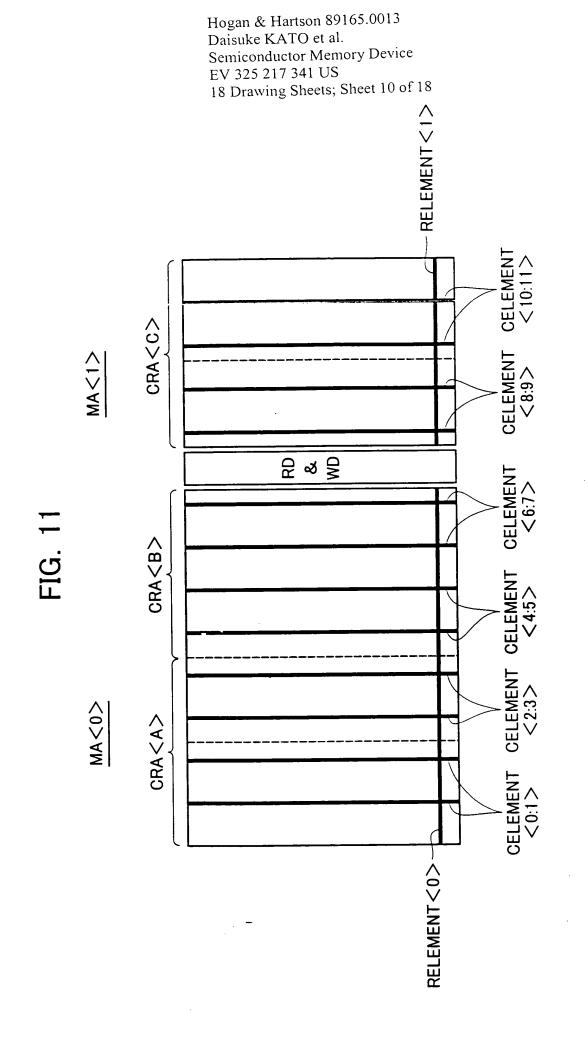
FIG. 8



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Hogan & Hartson 89165.0013 Daisuke KATO et al. Semiconductor Memory Device EV 325 217 341 US 18 Drawing Sheets; Sheet 9 of 18 RELEMENT<1> CELEMENT CELEMENT CELEMENT <6:7> <8:9> <10:11> CRA<C> MA<1> FIG. 10 CRA<B> B & B CELEMENT CELEMENT CELEMENT <0:1> <2:3> <4:5> MA<0> CRA<A> RELEMENT < 0 > --



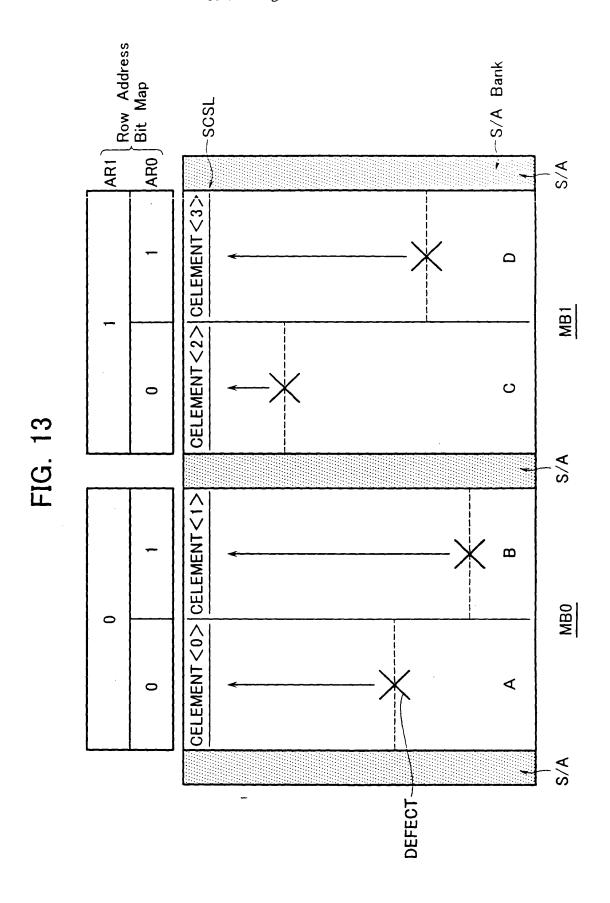
EV 325 217 341 US 18 Drawing Sheets; Sheet 11 of 18 <2>AA 0 0 <1>AA 0 0 ļ 0 0 ļ <0>AA 0 10 0 0 0 0 10 0 QSEG<7> SCSL (16+2) QSEG<6> QSEG<5> RELEMENTA < 0:n > QSEG<4> Parity DSEG<0> Parity DSEG<1> 8 & Q QSEG<3> SCSL (16+2) QSEG<2> MA<0> RELEMENTA < 0:n > QSEG<1> QSEG<0> (16+2)Mbit Normal Array Redundant Row Array Activated Sub Array Activated Sub Array 16 Sub Array

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Semiconductor Memory Device

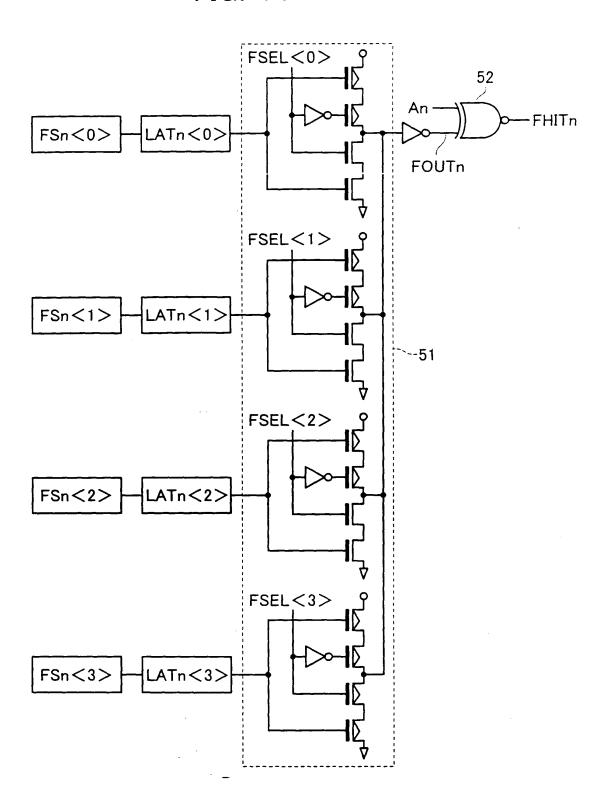
Daisuke KATO et al.

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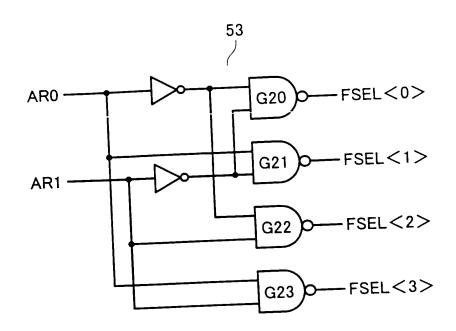
Hogan & Hartson 89165.0013 Daisuke KATO et al. Semiconductor Memory Device EV 325 217 341 US 18 Drawing Sheets; Sheet 13 of 18

FIG. 14



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FIG. 15



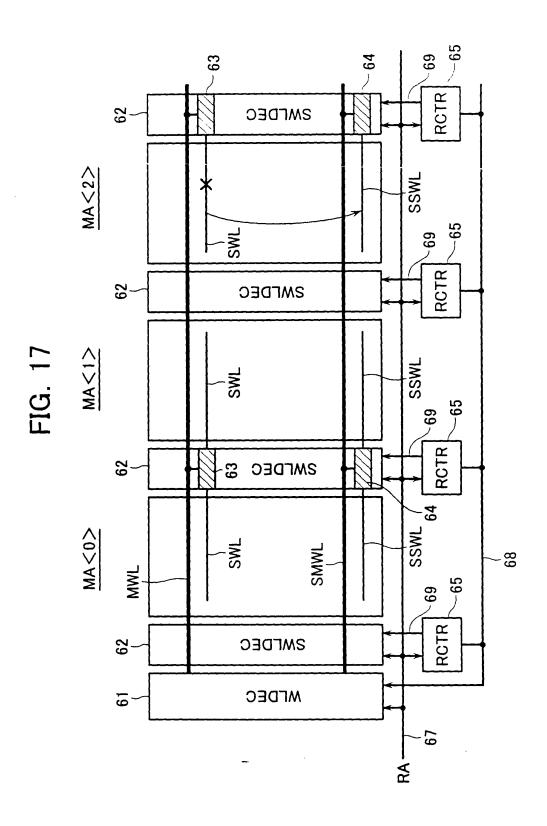
EV 325 217 341 US NS SWL Sheet 12 of 18 SSWL SWL SWLDRV RRA<e> SWL SWL SSWL RELEMENT < B > **SWLDRV** RRA<c> SWL RRA<b>> CRA RELEMENT < A > SSWL **SWLDRV** CELEMENT RRA <a> SWL RRA < d> SSWL MWL SWLDRV FIG. 16A

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FIG. 18

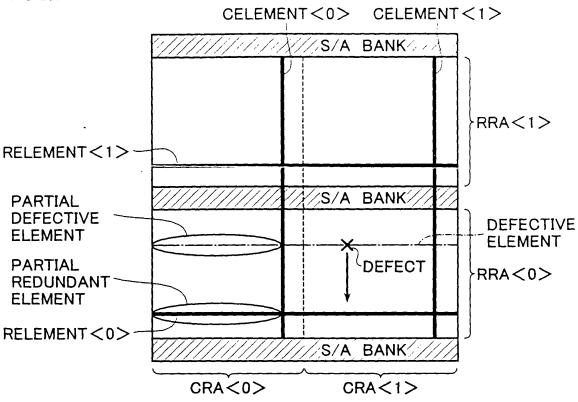
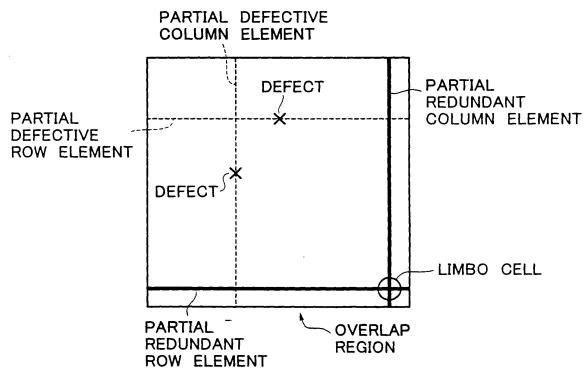


FIG. 19



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